

SiP Emerges

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The growth of System-in-Package (SiP) is the long-awaited renaissance in multichip packaging solutions, representing one of the largest growth markets in the electronic packaging industry. What is a SiP? How does it differ from the multichip packaging solutions first introduced decades ago? What are the key applications for SiP and what are the major drivers? Read on to learn the answers to these questions.



MCMs and MCPs

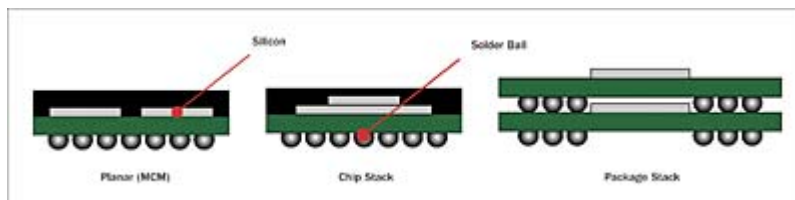


Figure 1. Package constructions for SiP

(Source: TechSearch International Inc., adapted from SiP Consortium and Sumitomo Bakelite).

When multichip modules (MCMs) were first introduced they were confined to high-end applications, where the value they contributed was large enough to absorb the cost of the necessary custom design, assembly, and test. Such applications include high-end computers, military, and aerospace applications.

The next generation application saw a transition to a few chip package known as a multichip package (MCP). The MCP appeared to be a low-cost solution because it used existing die and package structures, making use of the established packaging and assembly infrastructure. The most promising MCPs were functional blocks incorporated into applications such as fax modems. Despite countless conferences and thousands of published papers, a high-volume solution to drive down the cost of these MCPs remained elusive. In addition, the unavailability of known good die and the existence of test issues constrained broad market acceptance. Silicon integration almost always proved to be the winning solution for the products of the day.

The benefits of incorporating more than one die on a substrate are numerous and compelling. Multiple chip solutions provide better performance through shorter interconnects when compared to single chip packages connected through the printed circuit board (PCB) fabric. They have lower inductance, capacitance, crosstalk, and power consumption.

Multiple chip solutions greatly simplify the complexity of the PCB structure by relieving both local and global wiring issues. The number of layers needed in a PCB is a function of the pitch and pin count of individual components, the number of components on the board, and the feature sizes that must be utilized to meet performance specifications. Increasing I/O and decreasing component pitch drive layers into the board for escape. Plated through holes are used to connect the layers which in turn block the area under the component for other wiring. Global wiring, which creates the signal paths between components, is hampered by the blockage that can, in turn, add even more layers. By removing the components from the board, much of the wiring takes place in the package resulting in fewer through holes and layers in the PCB.

SiP Emerges

Recently a new generation of packaging for multiple chips has emerged. SiPs deliver increased functionality and performance in small form factor, resulting in significantly greater adoption rates than any previous multichip module. SiP solutions are increasingly found in a broad range of market segments, including consumer electronics such as digital cameras and camcorders, automotive, military/aerospace, medical, computer, and telecommunications products. With a unit growth rate of almost 20 percent CAGR between 2004 and 2009, semiconductor designers and fabs, along with substrate providers, assembly houses, circuit board manufacturers, EMS companies, and systems houses are experiencing changes brought about by the increased use of SiP. (Ref. 1).

What's a SiP?

SiP is a functional system or subsystem assembled into a single package. It contains two or more dissimilar die, typically combined with other components such as passives, filters, antennas, and/or mechanical parts. The components are mounted together on a substrate to create a customized, highly integrated product for a given application. SiPs may utilize a combination of advanced packaging including bare die (wire bond or flip chip), wafer level packages, pre-packaged ICs such as CSPs, stacked packages, and/or stacked die. A SiP can by definition be an MCM or MCP but the converse is not necessarily true. The fit depends on the type of devices being packaged and whether the result creates a functional block.

Table 1. Comparison of Package Shape and Characteristics. (Source: Renesas Technology).

Item	Stacked Die	Planar	PoP	QFP
Merit	Small size and high package density	High reliability with good thermal dissipation	Memory capacity copes with shrinkage	Easy to install, low cost
Miniaturization, high density	Excellent	Fair	Good	Fair
Thermal dissipation	Good	Excellent	Good	Good
Cost	Good	Fair	Fair	Excellent
Reliability	Excellent	Excellent	Good	Excellent
Test	Excellent (Renesas internally developed package)	Excellent	Good	Excellent

A diverse set of structures and configurations for SiP solutions has developed to meet the needs and drivers of the various market segments. Planar structures incorporate multiple devices on a single layer. The die may be directly attached to the substrate (direct chip attach) or packaged first, usually in a chip scale configuration.

3D packages feature die stacked in a Z direction. The die may or may not be inside packages (see Figure 1). A variety of configurations and interconnect methods have been developed.

There are essentially three types of 3D constructions utilized in SiP solutions. They are as follows:

1. A stacked die package consists of more than one die connected by wire bond, flip chip, or TAB to a substrate. The die stack may contain memory or memory and logic. Spacers may be used between die of the same size. With the inclusion of logic, the package can be considered a SiP.
2. A stacked package also called PoP is a construction of individual packaged die (usually in CSP format) that are stacked and interconnected to a substrate usually by wire bonding, flip chip, or tape automated bonding (TAB). The stacked package may consist of memory devices or a combination of memory and logic. When the stacked package includes logic, it can be considered a SiP.
3. Package-in-package consists of two or more packages assembled together and overmolded so that the end result is a single package that interconnects to the product board.

A comparison of the various SiP package shapes and characteristics from is found in Table 1.

SiP Adoption

In terms of unit volumes, the SiP has already seen greater success than any previous multichip packaging version. The demand for mobile phones and other portable products, such as digital cameras and camcorders, has driven the need for increased functionality and performance in a smaller form factor. Figure 2 shows the reasons for SiP adoption by customers of Renesas. (Ref. 2).

The advantages of SiP solutions include smaller form factor, faster turn-time, low NRE costs (compared to a single die design), and the ability to integrate heterogeneous technologies such as digital and RF. (Ref. 3).

SiP Applications

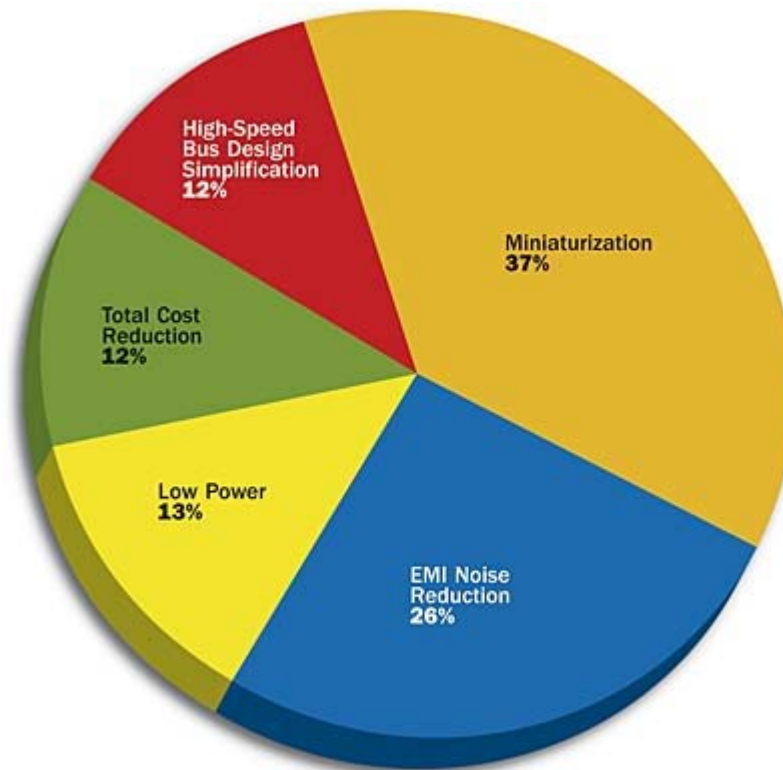


Figure 2. Reasons for adopting SiP

(Source: Renesas Technology).

There is a broad application space for SiP across many market segments, including consumer products such as digital cameras, camcorders, mobile phones, a variety of other wireless devices, automotive, military/aerospace, medical, computer, and telecommunications products. The many different structures seen in Table 2 reflect the particular needs and drivers of the end market.

A variety of SiPs are found in the RF, digital baseband, and transceiver sections of mobile phones. Power amplifiers (PAs) are considered SiPs. The trend towards increased use of modules for PA packaging will continue, driven by form factor and cost-reduction requirements. Many modules are as small as 4 mm x 4 mm, and PA modules incorporating antenna switch elements and some filters as well as matching elements, are common.

An increasing number of RF modules will be shipping as SiP configurations. SyChip has a module that incorporates integrated passives into the thin-film-on-silicon substrate. Flip chip devices are mounted on the module to provide a "plug and play" solution for a WLAN application. The module provides a complete system without the need for any external components or customer RF expertise. Philips and STMicroelectronics have also developed thin-film-on-silicon modules that incorporate passive devices in the substrate for a variety of products. Modules are shipping with both wire bond and flip chip mounted devices.

The baseband section of many of today's mobile phones also contains SiPs. Configurations include direct die stacking, package-on-package (PoP), and package-in-package (PiP) or stacked module packages. Intel uses a PoP structure with a folded flex circuit solution for an application processor and memory configuration. Texas Instruments (TI) ships a digital baseband and SRAM stacked die package configuration that is found in a number of phones.

Digital camcorder manufacturers have been early adopters of new and innovative packaging technology, and SiP is no exception. Driven by goals of smaller size and lighter weight, makers of cameras and camcorders continue to use advanced packages, including SiPs. Hitachi/Matsushita Electric Industrial jointly developed a camcorder using an SiP with stacked chips. Sony describes its SiP solution as "System Integrated Packaging." Its DCR-IP220 model contains a stacked package with logic and 128M SDRAM in a 240-pad array package. The DSC-F77 Cyber-Shot digital camera has also been introduced with SiPs. (Ref. 4). Sony has also introduced PoP solutions.

MP3 players are increasingly using SiPs. The mini disk drives in these consumer products utilize SiPs. These drives may also be found in future mobile phones.

SiPs are also used in computing and telecommunication systems. High-end computers from IBM and Hitachi along with midrange, and UNIX-based servers continue to use MCMs. Stacked packages and SiPs can also be found in blade servers. While the high-end systems typically feature bare die flip chip mounted on a complex, high-density substrate, and some configurations feature a bare die surrounded by packaged memory. Graphics modules are increasingly shipping with a processor surrounded by packaged memory. Cisco plans to use an SiP in its future network systems. Its design allows reduced layer counts in the system board and total system cost savings. (Ref. 5).

SiP applications also include medical electronics, such as smart pills and implantables, along with automotive, defense electronics, and aerospace applications. While these applications represent smaller unit volumes, they account for high dollar values. New camera modules will feature SiPs. Solid-state lighting, home electronics, and other systems are also expected to make use of SiPs.

Key Issues for SiP

Chip-scale packaging was one of the key enabling technologies for the emergence of SiP. The ability to package die in near chip-size footprints, along with the development of stacking techniques, yields alternatives to MCM and MCP solutions. However, the new technology also introduces new concerns, including logistical and engineering issues, wafer thinning, and assembly. Handling of thin die can be challenging for the assembler who must take great care during the attachment and bonding processes to avoid damage. The availability of bare die continues to be a problem. The issue of KGD is one of the reasons for the development of the PoP and PiP configurations. (Ref. 6).

Table 2. SiP Constructions. (Source: TechSearch International, Inc.)

Company function (structure)	Die	Package type, body size (mm)	Lead count	Interconnect method	Ball pitch (mm)
SyChip RF module (planar)	3 (base band processor, RF transceiver, EEPROM)	Laminate QFN footprint 12.6 x 15.8	60	Wire bond	0.7
SyChip RF module (planar)	4 (base band, EEPROM, RF transceiver/receiver, GaAs switch)	Chip scale 9 x 9, 10 x 10	47	Flip chip	0.8
Skyworks Radio module (planar)	6 (transceiver, PA, switchplexer, controllers)	LGA 13 x 13	40	Wire bond	0.5 - 1.0
Freemcale Baseband module (stacked)	3 (base band, PSRAM, flash)	PBGA 13 x 13	225	Wire bond	0.8
Intel (PoP)	3 (processor, flash, SDRAM)	BGA 14 x 14	336	Wire bond	0.65
Sony (stacked die)	2 (CPU, flash)	PBGA 12 x 12	304	Wire bond	0.5

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SiP solutions represent a merging of first (chip to package) and second (package to board) level packaging. Many of the challenges the industry faces have been addressed by PCB fabricators and EMS providers. For example, SiP

structures present new issues in design. Models and algorithms developed for single chip solutions cannot accommodate the electrical, thermal and mechanical issues introduced with multiple die. New test strategies for these complicated structures are also a major hurdle. SiP packaging solutions, which require managing both packaged and bare die from multiple sources, introduce the type of supply chain problems that have been conquered by EMS companies.

Conclusions

SiP is indeed the rebirth of a concept that has been with us for many years, first as MCM and then as MCP. Developments in assembly process technology as well as new market drivers have led to a renewed interest. Initially the solutions that focused on incorporating like-function did not meet the true definition of a system. However, it is impossible to ignore these packages in our discussions because of many overlapping benefits and concerns. In addition, the SiP concept has already evolved to include these stacks as a piece of a more highly integrated functional block. SiP is one of the fastest growing packaging solutions. Its adoption creates new opportunities for market entry and challenges across the entire supply chain.

SiP is changing the way the industry approaches packaging. Solutions must be considered in the planning stage of system design as an integral part of the overall strategy. System design processes must change to achieve this. The electronics industry has migrated to a structure where design skills are decentralized and located in many separate companies. It is imperative that system architects, IC designers, I/O planners, packaging engineers, printed circuit board designers, and manufacturing in all disciplines be provided the means to work closely together. Virtual reintegration across the supply chain is critical to enable co-development and co-design.

TechSearch International's 142-page report "System-in-Package, The New Wave in 3D Packaging," can be purchased by visiting www.techsearchinc.com.

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